ABSTRACT OF THE DISCLOSURE

Disclosed herein is an organization of cache memory for hardware acceleration of the FDTD method. The organization of cache memory for hardware acceleration of the FDTD method provides a substantial speedup to the finite-difference time-domain (FDTD) algorithm when implemented in a piece of digital hardware. The organization of cache memory for hardware acceleration of the FDTD method utilizes a very high bandwidth dual-port on-chip memory in a particular way. By creating many small banks of internal memory and arranging them carefully, all data dependencies can be statically wired. This allows for a many-fold speedup over SRAM-based solutions and removes the burden of data dependence calculation that streaming SDRAM-based solutions must perform.